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An Interrelated Current-Voltage/Capacitance-Voltage Traces-Based Characterisation Study on 4H-SiC Metal-Oxide-Semiconductor Devices in Accumulation and Si Device in Inversion Along With Derivation of the Average Oxide Fields for Carrier Tunnelling From the Cathode and the Anode

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Abstract: *The equations for the average oxide fields for carrier tunnelling across the metal-gated MOS devices in accumulation and having charges in the oxide have been derived in this article. It has been clarified that N incorporation in the oxide by NO annealing at 1150 or 1175^oC for 2 hrs does not affect the MOS characterisation as N is incorporated only at the SiC/SiO_2 interface within the 2 nm of the interface and the flat band voltages remain the same before and after NO annealing. Both, dry and wet oxidation which includes wet re-oxidation anneal at 950^oC for 3 hrs(ROA) followed by N incorporation due to NO annealing, give reproducible flat band voltage (V_{fb}) values as shown in studies by different research groups. However, NO annealing reduces the interface trap density (D_{it}) by at least one order by passivating the defects at the SiC/SiO_2 interface. A new method of finding the density of near interface traps in n-4H-SiC and Si MOS device is proposed from the observed low field leakage current. The density of NITs in the oxide at 300 K is found to be 23.5 x $10^{11}/cm^2eV$ on 4H-SiC and 12 x $10^{11}/cm^2eV$ on Si near the CB edge. Only the oxide on SiC is NO annealed. The study of the low and high field I-V traces relative to the displacement current of the oxide informs us about the border trap density and bulk defect density. The barrier height dependent breakdown in SiO_2 on 4H-SiC is lower than on Si for both electrons and holes as current carriers.*

Keywords: *Cathode, FN- tunnelling, Metal-Oxide-Semiconductor, Silicon, Silicon Carbide*

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I. Introduction

Fowler-Nordheim (FN) hole tunnelling across a MOS device has been demonstrated by many groups to date [1-15] with the early speculation in1976 [1, 2] for the phenomenon. Weinberg et al. [1] proposed possible hot hole injection from the silicon valence band into the SiO_2 and obtained a small value for hole effective mass in the oxide of 0.31m, where m is the free electron mass. Rai et al. [2] proposed possible double injection into the oxide to explain instability in the current through the oxide at high fields. Hole injection by internal photoemission has also been shown to occur at the silicon nitride/Si interface [16] and 4H- and 6H-SiC/SiO_2 interface [17]. The hole effective mass in amorphous SiO_2 has been determined to be 0.58m, where m is the free electron mass [8, 18, 19]. The hole effective mass in the crystalline form of SiO_2 called beta-cristobalite, having a bandgap of 8.76 eV, has also been determined to be 0.58m by looking at the conduction band maximum at the Brillouin zone boundaries where there are hole states [20]. The electron effective mass in SiO_2 is already accepted to be 0.42m [7, 19, 21-24]. These two values bring to the notice that the electron and hole effective masses add to the value of free electron mass for the amorphous insulators. This unique feature is clubbing all amorphous insulators together. The feature is quite intriguing and requires only one of the masses to be determined.

II. Derivation Of The Average Oxide Fields

A simple structure of metal-gated metal-oxide-semiconductor (MOS) in accumulation is shown in Fig.1 below with oxide of thickness d between cathode and anode. A uniform sheet of positive charge is shown at a distance a, from the cathode that causes cathode field enhancement and anode field reduction [18, 25]. A sheet of negative charges in the oxide would cause cathode field reduction and anode field enhancement. The cathode field E_1, and the anode field E_2 derivation using Gauss's law has been presented in the earlier study by revisiting Klein's study of 1972 [18, 25]. The derivation for the average oxide field for electron tunnelling from the cathode and hole tunnelling from the anode had been left for the reader to derive in the earlier study [18].

The earlier study is now extended by presenting the derivations of the average oxide fields for carrier tunnelling. It is to be noted that the I-V characteristics across the MOS device in accumulation has originated in the works of J. S. Townsend in the early 20th century [26], when he was studying electricity in gases. The gases at low pressure were acting as the dielectric then, which in the MOS device is replaced by amorphous SiO_2.

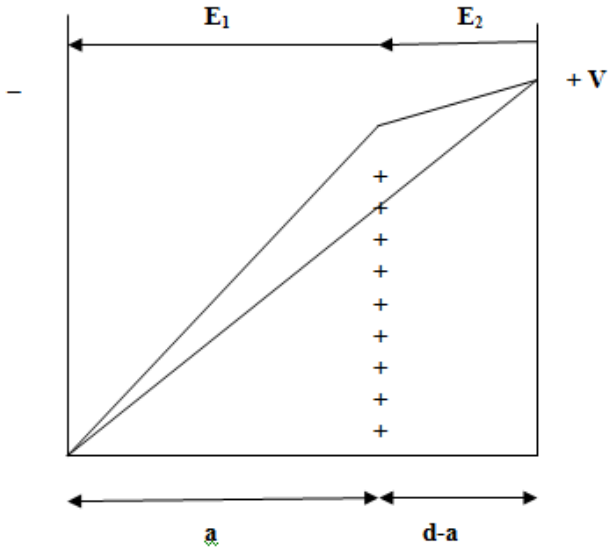

Fig. 1 The oxide of thickness d between cathode and anode having V volts applied across them. A uniform sheet of positive charge at a distance a, from the cathode causes enhancement of the cathode field E_1 and reduction of the anode field E_2.

Consider electron tunnelling from the cathode of a MOS device having positive charges in the oxide at a distance a, from the cathode. The oxide thickness is d and the applied voltage across the device is V. Let X be the gate bias for which the cathode field E_1=F, where F is the applied field across the device without charges in the oxide. Then,

$X= E_1a + E_2(d-a)$ (1)
$E_1=E_2 + \sigma F$ (2)
$E_2=E_1-\sigma F$
$E_2=F - \sigma F$
$X=Fa + (F-\sigma F)(d-a)$
$X=aF + dF – aF – \sigma F(d-a)$
$X=dF – \sigma F(d-a)$
$X=dV/d – (\sigma V/d) (d-a)$
$X=V – \sigma V ((d-a)/d)$

If a uniform distribution of charges is assumed in the oxide as a simple case of charge distribution because traps are present throughout the oxide, then the centroid of the charges will be at a =d/2. Then,

$X=V – \sigma V/2$ (3)

A modelling study by Miranda et al. [27] provided the relation between flat band voltage V_{fb}, and the oxide charge density for the case of uniform distribution of charges. It is given by:

$$\rho_{ox} = (2\epsilon_{ox} \mid \Delta V_{fb} \mid) / t_{ox}^2, \quad (4)$$

where ρ_{ox} is the oxide charge density, ϵ_{ox} is the permittivity of the oxide, ΔV_{fb} is the change in flatband voltage only due to the charges, and t_{ox} is the oxide thickness which is same as d in Fig. 1.

Here, $\Delta V_{fb} = V_{fb} – W_{ms}$, where, W_{ms} represents the ideal V_{fb} for the MOS device without charges in the oxide. ΔV_{fb} represents only the charges in the oxide.

Also, stored charge $Q = (\epsilon_0\epsilon_r A\ V) / t_{ox}$. (5)

Positive charge density per unit volume, $\rho_{ox} = (\sigma Q) / (A\ t_{ox})$

$$\rho_{ox} = (\sigma\ \epsilon_0\ \epsilon_r\ A\ V) / (A\ t_{ox}\ t_{ox})$$

Substituting for ρ_{ox}, we get, $(\sigma\ V/2) = \mid \Delta V_{fb} \mid$.

In the above derivation only the oxide charges represented by ΔV_{fb} have been considered. Actually,

$$V_{fb} = W_{ms} – (Q_f + Q_{ot} + Q_{mo} + Q_{it})/ C_{ox}. \quad (6)$$

Here, Q_f, Q_{ot}, Q_{mo}, and Q_{it} represents the fixed oxide, oxide trapped, mobile ionic, and interface trapped charge densities. C_{ox} is the oxide capacitance per unit area, and W_{ms} is the metal-semiconductor work function difference. Q_{it} becomes part of the V_{fb} when the interface trap density is very high, of the order of 10^{12} $cm^{-2}eV^{-1}$ or greater. Therefore, V_{fb} obtained from the C-V measurements, that includes the effect of all the above charges and W_{ms} has been used in the calculations of oxide voltages and average oxide fields, F_{av}. A negative measured value of V_{fb} on the C-V curve signifies net positive charges in the MOS device including W_{ms}, and a positive measured value of V_{fb} on the C-V curve signifies net negative charges in the MOS device including W_{ms}.

$$\sigma V/2 = \left| V_{fb} \right| \text{ when } W_{ms} \text{ is included.} \qquad (7)$$

Now, subtracting V_{fb} from V gives only the oxide voltage. So, the voltage across the oxide,

$$V_{ox} = \left| V \right| - \left| V_{fb} \right|. \qquad (8)$$

The average field across the oxide in the MOS device having positive charges in the oxide, for electron tunnelling from the cathode is now given by:

$$F_{av} = (\left| V \right| - \left| V_{fb} \right|) / d \qquad (9)$$

Similarly, consider hole tunnelling from the anode of a MOS device having positive charges in the oxide at a distance a, from the cathode. The oxide thickness is d and the applied voltage across the device is V.
Let X be the gate bias for which the anode field E_2=F, where F is the applied field across the device without charges in the oxide. Then,

$X=E_1a + E_2 (d-a)$
$E_1=E_2 + \sigma F$
$E_1=F + \sigma F$
$X= (F + \sigma F)\, a + F\, (d-a)$
$X= aF + a\sigma F + dF - aF$
$X= dF + a\sigma F$
$X= dV/d + a\sigma V/d$

Once again, for a simple case of a uniform distribution of charges in the oxide, the centroid of the charges will be at a=d/2. Then,

$$X= V + \sigma V/2 \qquad (10)$$
$\left| V_{fb} \right| = \sigma\, V/2$ as shown earlier.

V_{fb} includes W_{ms}. Therefore, adding V_{fb} with V gives only the oxide voltage. So, the voltage across the oxide is given by:

$$V_{ox} = \left| V \right| + \left| V_{fb} \right|. \qquad (11)$$

The average field across the oxide of a MOS device having positive charges in the oxide, for hole tunnelling from the anode is given by:

$$F_{av} = (\left| V \right| + \left| V_{fb} \right|)/d \qquad (12)$$

The derivations of the average field across the oxide for the two cases of electron and hole tunnelling having positive charges in the MOS devices are presented above with the average fields given by equations (9) and (12). Similar derivations of the average oxide fields can be performed for electron and hole tunnelling in the MOS devices having negative charges in the devices. The oxide voltages for all four cases have already been presented in the author's earlier study [8, 18]. The use of the phrase 'positive charges in the MOS device' means that W_{ms} is included with the charges in the oxide.

III. Discussion

FN electron and hole tunnelling in metal-gated n- and p- type 4H-SiC MOS devices having oxides grown on the Si-face of exactly 40 nm were demonstrated in the year 2000 by the author in collaboration with Auburn-Vanderbilt experimental group in USA [8]. FN electron tunnelling occurred from the cathode of the n-type MOS device in accumulation with Mo gate and FN hole tunnelling occurred from the anode in two p-type MOS devices in accumulation with Au and Mo gate with a small difference in the two hole tunnelling currents due to the difference in the work functions of Au and Mo gates. The n-4H-SiC conduction band offset (CBO) on the Si-face was determined to be 2.78 eV using the accepted electron effective mass value of 0.42m for SiO_2

from the Mo-gated n-type MOS device [8]. The hole effective mass in SiO_2 was determined to be 0.58m using 2.9 eV valence band offset (VBO) for the p-type MOS device with Au gate [18]. The oxides of the devices were grown by wet oxidation at 1100^{o}C [28] to a thickness of 36 nm, and annealed in NO at 1150^{o}C for 2 hours with additional oxidation of 4 nm to give the total oxide thickness of exactly 40 nm. The wet oxidation process includes a wet re-oxidation anneal at 950^{o}C for 3 hrs (ROA) that does not grow oxide any further but changes the oxide effective charge and thus the V_{fb} [29, 30]. A similar change in V_{fb} is also seen in dry oxidised MOS device after ROA [31].

A. Reproducible flat band voltages

Section II above presents the derivation of the average oxide fields in the MOS devices. It can be observed that the non-reproducible V_{fb} under similar processing conditions of the MOS devices can change the oxide fields and can give erroneous FN parameter values. Various studies on 4H-SiC MOS devices have been tabulated in Table I below. It can be observed that, for both dry and wet oxidised MOS devices having ROA as part of the oxide growth process, V_{fb} is reproduced, as that in the author's earlier study [8, 18] of -6 V on the p-type device and less than 1 V on the n-type device, keeping the gate metal work functions in mind. The use of Au gate having a work function of 5.1 eV shifts the C-V curve for the p-type device to the left by 1 V, as compared to the device having Al gate having a work function of 4.1 eV, for hole conduction [32]. The C-V curve for the n-type device having Mo gate shifts to the right by 0.6 V for electron conduction, as compared to the device having Al gate [32, 33], and reproduces V_{fb} of less than 1 V. The references of various studies are given in the first column in Table I.

Table I. Flat Band Voltages (V_{fb}), in n- and p- type 4H-SiC MOS devices having different oxide growth and annealing conditions. The MOS devices have different gate metals. Wet re-oxidation at 950^{o}C for 3 hrs is denoted by ROA, which is usually part of the oxide growth process.

Row. [Ref]	4H-SiC-MOS	oxidation	NO anneal, Temperature, time	Oxide thickness (nm)	Gate metal, work function (eV)	V_{fb} without ROA (Volts)	V_{fb} with ROA (Volts)
1.[8, 18]	p-type, author	Wet, 1100^{o}C	1150^{o}C, 2hr.	40	Au, 5.1 eV		-6 V
2.[30]	p-type	Wet, 1150^{o}C		50	unknown	-9.95 V	-4.26 V
3.[31]	p-type	Dry, 1200^{o}C		35-45	p-poly-Si, 5.2 eV	-7.5 V	Close to - 6V
4.[32]	p-type	Dry, 1150^{o}C	1175^{o}C, 2hrs		p-poly-Si/Al bilayer, 4.1 eV		-5.0 V, less than -6 V due to gate metal
5.[8, 18]	n-type, author	Wet, 1100^{o}C	1150^{o}C, 2hrs	40	Mo, 4.7 eV		Less than 1V
6.[32]	n-type	Dry, 1150^{o}C	1175^{o}C, 2hrs		p-poly-Si/Al bilayer, 4.1 eV		-0.5V, negative due to gate metal
7.[33]	n-type	Dry, 1150^{o}C	1175^{o}C, 2hrs	45	Mo/Au bilayer, 4.7/5.1 eV		Slightly positive but, less than 1 V

B. Nitrogen incorporation at the SiC/SiO_2 interface does not change V_{fb} at room temperature

Nitric oxide (NO) annealing at 1150 or 1175^{o}C is performed for 2 hrs that incorporates nitrogen at the SiC/SiO_2 interface after the oxide growth process. The oxide growth process includes ROA. The N at the interface passivates the defects and reduces interface trap density (Dit) by one order [34], but does not change the V_{fb} for both n- and p-type MOS devices [35, 36]. It grows some oxide further of about 4 nm at the rate of 2 nm / hr. It has been shown that N incorporates only at the SiC/SiO_2 interface within about 2 nm, without affecting the bulk of the oxide [37-40]. Prof. L.C. Feldman of the experimental group [8, 18], had expressed concern about N incorporation in the oxide affecting the MOS characterisation. In particular, if the V_{fb} value is not reproducible, then the oxide fields will change for different experiments. This has been clarified in the above sub-section A and in the present sub-section B, that it does not affect the MOS characterisation, provided ROA is part of the oxide growth process. This was also supported by the MOS characterisation utilising n^+ polysilicon gated n-channel Si MOSFET that yielded the hole effective mass in the oxide as 0.58m [19]. Here the Si/SiO_2 interface did not have any N and the band offsets were also vastly different and had a different V_{fb} . The oxide thickness needs to be exact in the determination of FN parameters [41]. The capacitor dot diameter was 340 μm [28], giving the dot area of 9.1 x 10^{-4} cm^2 instead of 10^{-3} cm^2 mentioned approximately in the study [8, 18]. However, the dot area can be ignored for the determination of FN parameters [41].

C. Significance of the SiO_2/n-4H-SiC(0001) Si-face interface barrier of 2.78 eV

The above interface barrier height has been reproduced for both grown and deposited oxides on 4H-SiC [42-45]. In particular, Ouennoughi et al. [42] mentions in Table I of their study that Si-face 4H-SiC/SiO_2 CBO

of 2.78 eV is reproduced by their group on the N_2O grown SiO_2 having a thickness of 90 nm [43]. The above reproducible CBO indirectly confirms that the oxide thickness must be exactly 40 nm in the author's earlier study along with the V_{fb} value of less than 1 V for the n-type device because a thickness of 40 nm was used in the calculations to yield 2.78 eV CB barrier height [8]. An earlier study by Afanasev et al. [46] reported the top of the valence band in all polytypes of SiC to be at 6 eV from the oxide conduction band. This study was based on internal photoemission of electrons from the semiconductor into the oxide. For the known 4H-SiC experimental band gap of 3.23 eV [47] that reduces the intrinsic value of 3.27 eV by 40 meV due to doping, yields the conduction band offset of 2.77 eV.

D. Positive charge build-up due to measurement delay, increases electron current and the CBO

A constant voltage stress study has been performed on n^+ poly-Si/SiO_2/4H-SiC(0001)Si face MOS device in accumulation [43]. It has been observed that the positive charge builds up with the stress time at about 8.5 MV/cm. This stress time is the measurement delay time for the next C-V measurement. It increases the electron current in the device and therefore increases the CBO and also creates a hump in the I-V characteristics starting from about 7.5 MV/cm due to positive charging. This effect does not happen with the author's earlier study [8, 18]. I-V characteristics in the samples of the author's study have a virgin I-V pass on the MOS devices in accumulation with a ramped voltage of 1V/s for the n-type device and 0.5V/s on the p-type device. I-V curves were obtained on many C-V dots. One representative I-V curve for the devices was shown in the figure. There is no hump in the I-V characteristics and hole injection in the p-type device starts at 7.2 MV/cm due to FN hole tunnelling. A similar constant voltage stress study has also been done on NO annealed Al/SiO_2/n-4H-SiC (0001) Si MOS device in inversion with holes injected from the anode [48]. Here again, the increase in measurement delay which is proportional to the increase in injected hole density shows an increase in positive charge build up and the V_{fb} shifts to more and more negative values. In both the CVS based studies [43, 48], the positive charge build up is more for N containing oxide. The constant voltage stress is different from applied ramp voltage as in the author's earlier study [8, 18] where the positive charging is very small, particularly at low fields, as discussed further in the next sub-section.

E. All NITs in the oxide fill with electrons with the n-MOS device in accumulation and lowers leakage current

When one observes the low field leakage current in the n- and p-type 4H-SiC MOS devices in accumulation in the author's earlier collaborative study [8], the currents are 8×10^{-13} A for the n-type device and 8×10^{-12} A for the p-type device. The oxide capacitance in accumulation is 78 pF for the 40 nm oxide having a C-V dot area of 9.1×10^{-4} cm^2 . The C-V dot diameter is 340 μm [28]. If one calculates the displacement current for the 78 pF oxide capacitance with the low frequency ramp rate of 0.1 V/s, the current comes out to be 7.8×10^{-12} A. This current is same as the observed current in the p-type device meaning that this is the leakage current for the oxide only. The observed current in the n-type device is one order lower because the near interface traps (NIT) are trapping electrons and storing charge thereby reducing the current. The low frequency capacitance is given by;

$$C = I / (dV/dt) \qquad (13)$$

The CB of n-4H-SiC MOS device is at the Fermi level E_F at accumulation bias of about 0.2 V equal to average electron energy of 0.2 eV. The NITs are inside the SiO_2 layer and can exchange charge with the 4H-SiC CB as border traps [49] for a small-signal ac voltage, or can be charged with electrons at positive applied ramp bias at the gate. The ramping is really not necessary for trapping at NITs. It is required for obtaining the I-V trace with the MOS device in accumulation. The NITs have a energy barrier of 0.2 eV which the electrons in accumulation are able to cross. Also, the electron concentration in the semiconductor has become equal to the density of states in the CB of $1.7 \times 10^{19}/cm^3$ at 300K for 4H-SiC when E_c minus E_F equals zero in accumulation, and the semiconductor becomes like a metal with high concentration of electrons having 1 nm thickness. The exponential distribution of electron concentration has now become equal to 1 in accumulation and it is known that N_C has $aT^{3/2}$ dependence for three degrees of freedom. This can be inferred from the concentration of electrons in the CB, n, given by the formula as;

$$n = N_C \exp\left(-\frac{E_C - E_F}{kT}\right) \qquad (14).$$

Here, N_C is the density of states in the CB of the semiconductor 4H-SiC, E_C is the bottom of the CB, E_F is the Fermi level of the doped semiconductor, 4H-SiC, k is the Boltzmann constant, and T is the temperature in Kelvin.

The ramp rate will capture electrons into the traps in the oxide and charge them. The low frequency limit of the ramp rate is 0.1 V/s at which all the traps are able to respond except traps with very large trap time constant of more than 1s and above. This ramp rate therefore brings out the total trap capacitance. Choosing a higher ramp rate would leave out more trap states to follow the signal and will therefore give a lower trap density. The capacitance determined from the equation (13) is 8 pF for the observed leakage current of 8×10^{-13} A and using

the ramp rate of 0.1 V/s for the n-type device having an oxide capacitance of 78 pF. This 8 pF is the equivalent series capacitance of the oxide and the capacitance, C_{NIT}, of the trapped near interface acceptor or electron traps [50]. C_{NIT} can be determined by;

$$(1/8\text{pF}) - (1/78\text{ pF}) = (1/C_{NIT}).$$

This gives C_{NIT} as 8.9 pF.

$$\text{Average } D_{NIT} = C_{NIT}/ (qA(kT)) \qquad (15).$$

Here, the area of the C-V dot is 9.1 x 10^{-4} cm^2 as mentioned earlier for a dot diameter of 340 µm. This gives average D_{NIT} as 2.35 x $10^{12}/cm^2$ eV for an average thermal energy of 0.026 eV at 300 K. This energy of 0.026 eV identifies the position of D_{NIT} at 0.026 eV from the CB edge. It is compared with trap densities away from the CB edge in the Table II below. It can be observed that at 0.1 eV from the CB in Williams et al. [51], D_{it} is 20 x $10^{11}/cm^2$ eV, and at midgap it is in low 10^{11} order. D_{NIT} obtained by the DC leakage current is 23.5 x $10^{11}/cm^2$ eV at 0.026 eV from the CB edge. D_{NIT} is found to increase as we get to sub-0.1 eV energy range to the CB edge.

Table II. D_{NIT} at 0.026 eV from CB edge in the present work compared with trap densities deeper in the CB.

Reference	Sample on n-4H-SiC (0001) Si-face	Oxide growth condition	NO anneal condition	Measurement method	Trap density at 300K ($cm^{-2}eV^{-1}$) (x 10^{11})	Location of traps from the CB edge
Chanana et al. [8]	Mo/SiO_2/n-4H-SiC	Wet ox at 1100°C with ROA	1150°C for 2 hrs	DC leakage current at low fields in accumulation	23.5	0.026 eV
Williams et al. [51]	Mo/SiO_2/n-4H-SiC	Dry and wet ox at 1100°C with ROA	1175°C for 2hrs	Hi-Lo C-V method	20	0.1 eV
Perez-Tomas et al. [52]	Al/SiO_2/n-4H-SiC	Dry ox at 1175°C with ROA	No NO anneal	Terman, Conductance and Hi-Lo C-V methods	20	0.1 eV
Potbhare et al.[53]	p-poly-Si/SiO_2/n-4H-SiC	Dry ox at 1150°C	1175°C for 2 hrs.	I_D-V_G, MOSFET, subthreshold slope	2.3	midgap
Pande et al.[54]	Al/SiO_2/n-4H-SiC	Dry ox at 1250°C	1250°C for 60 min	AC Conductance	8.0	0.13 to 0.23 eV
Jia et al.[55]	Al/SiO_2/n-4H-SiC	Dry ox at 1300°C	1175°C for 2 hrs.	Bidirectional HF C-V before stress	4.1	midgap
Poggi et al. [56]	Al/SiO_2/n-4H-SiC	Two step wet ox at 800°C and 1100°C	High N implant before ox in place of NO anneal	Hi-Lo C-V	4.0	0.3 eV

Basically, the high frequency C-V trace does not allow traps having large capture-emission time constants to follow the small-signal ac voltage and so these traps do not store charge, whereas the low frequency C-V trace allows all the traps but some very slow traps with capture-emission time constants of 1s or more to follow the small-signal ac voltage and so nearly all the traps store charge. Therefore, if one scans two traces at high frequency at the same temperature, say room temperature, and calculate the trap density based on change in voltage from the hysteresis, it will give a lower trap density as in the works of Jia et al. presented in Table II above [55]. The two traces are not including all the traps. Similarly, the works of Potbhare et al. [53] also mainly give the midgap trap density, and Poggi et al. [56] gives trap density at 0.3 eV from the CB edge, which is one order lower than that near the band edges.

The Effective mobility and Field Effect (FE) mobility in a MOSFET in inversion are the surface mobility due to the field effect. The effective mobility is derived from the channel conductance and the FE mobility is derived from the trans-conductance of a MOSFET device. They have been shown to be inversely proportional to D_{NIT} at low temperature of 11K by Yoshioka et al. [57] and directly proportional to the temperature by other research groups [52, 53]. The bulk mobility (Hall mobility) we know is proportional to $T^{3/2}$ for impurity scattering at low temperatures because of three degrees of freedom when the kinetic energy of electron is equal to 3/2 (kT). The surface mobility should then be proportional to 2kT/2 because of two degrees of freedom. This argument also supports direct proportionality of FE mobility to temperature. Therefore, it is inferred that D_{NIT} is inversely proportional to temperature at low temperatures such as 11 K when the semiconductor behaves like a metal and the carrier distribution is equal to N_C. N_C for two degrees of freedom is

proportional to temperature T in Kelvin. This means that D_{NIT} has a $(T/300)^{-1}$ relation which is the same as shown by equation (15) above. The D_{NIT} near CB are calculated from room temperature to 1 K based on equation (15) and tabulated below in Table III.

Table III. Distribution of D_{NIT} near the CB edge, and D_{it} near the VB edge.

Temperature, K	D_{NIT} near CB $cm^{-2}eV^{-1}$	D_{it} near VB $cm^{-2}eV^{-1}$	Location of traps from band edge, (eV)
300	2.35×10^{12}	7.7×10^{11}	0.026
100	7.05×10^{12}	2.31×10^{12}	0.0087
10	7.05×10^{13}	2.31×10^{13}	0.00087
1	7.05×10^{14}	2.31×10^{14}	0.000087

The D_{NIT} in the oxide near the CB of 4H-SiC presented in the Table III above, closely matches with those estimated values obtained by Cher Xuan Zhang et al. [58] in their study of the temperature dependence of 1/f noise of 4H-SiC MOSFETs. The samples used in the study by the author were similar to the MOSFETs [8], thereby corroborating the proposed method above. The increase of D_{NIT} at lower temperatures is corroborated by another study, where the high frequency C-V plot at 100K temperature shows an increase in 'stretch-out' of the C-V curve indicative of an increase in D_{NIT} [59]. This 'stretch-out' can be easily explained. A low temperature C-V curve includes charged traps closer to the band edges. The trapped charges are electrons at the CB edge and holes at the VB edge. Adding trapped electrons adds negative charges, and the C-V curve shifts right near accumulation on the n-type device. Adding trapped holes adds positive charges, and the C-V curve shifts left near inversion on the n-type device. These opposite shifts near accumulation and inversion regions of the n-MOS device, stretches the C-V curve indicating that the trap capacitance has increased. Lowering the temperature lowers the average thermal energy of electrons and is equivalent to obtaining D_{NIT} closer and closer to the conduction band edge. The study at 11K temperature determined the D_{NIT} for a n-channel MOSFET having NO anneal as $4.2 \times 10^{14}/cm^2eV$ [57]. This is about 6 times more than the value in the Table below at 10K temperature as $7.05 \times 10^{13}/cm^2$ eV. The method to determine the above trap density is by utilising the sub-threshold slope of the MOSFET's I_D-V_G characteristics. This method is different from the low voltage leakage current method of the present article and is known to give higher trap densities. The trap density of $7.05 \times 10^{13}/cm^2$ eV at 10K shown in the Table III above is nearly the same as $6 \times 10^{13}/cm^2$ eV at the band edge by Potbhare et al. [53]. This corroborates the low field leakage current method of finding D_{NIT} at sub-26 meV energy level from the CB edge. Similarly, raising the temperature can identify border traps away from the CB edge by raising the average electron energy to 0.048 eV at 557 K temperature [60]. Some slow states are left out when using the 1 MHz C-V plots, as compared to the leakage current method presented in this article, where the low frequency ramp rate includes all the NITs.

In the p-type device in accumulation, the low voltage leakage current observed is 8×10^{-12} A. The ramp rate for the device can be taken as 0.1 V/s, giving the overall capacitance is determined to be 80 pF. This is the oxide capacitance and therefore the current represents the displacement current of the oxide capacitance. There are no near interface traps at the VB edge. The D_{it} at E_v + 0.1 eV is obtained as $2 \times 10^{12}/cm^2$ eV before NO annealing [51], which reduces by one order after NO annealing to be $2 \times 10^{11}/cm^2$ eV. This density can be extrapolated to $7.7 \times 10^{11}/cm^2$ eV at 0.026 eV from VB edge by multiplying by a factor of (0.1eV/0.026eV). All the trap densities at lower temperatures up to 1 K are presented in the Table III above in column 3. The FN parameters are obtained at high fields, where the currents are much larger, and therefore the low field leakage current does not affect the determination of the FN parameters.

It can be observed from Table III above, that the trap density near the CB and VB edges in 4H-SiC MOS device after NO annealing are comparable and of the order of $10^{14}/cm^2eV$. Low voltage long time bias stress for 48 to 72 hrs or even one year [61] will cause change in threshold voltage in both the p-channel and n-channel MOSFETs due to Bias Temperature Instability (BTI). Negative bias temperature Instability (NBTI) will occur in the p-channel MOSFETs in inversion with negative voltage at the gate. Positive Bias Temperature Instability (PBTI) will occur in the n-channel MOSFETs in inversion with positive bias at the gate. In Si technology, the change in threshold voltage due to NBTI is more than due to PBTI for the current high-K metal gate (HKMG) technology [61, 62]. Similar observation is expected for the n-and p-channel 4H-SiC MOSFETs also. NBTI will cause a degradation of the threshold voltage on p-channel MOSFETs and PBTI on the n-channel MOSFET.

F. Improving electron mobility in n-channel 4H-SiC MOSFET

The author in collaboration with the experimental group [8, 18, 63] studied the effective mobility in an n-channel MOSFET on 4H-SiC. The resulting effective surface mobility for the device was a low value of about 35 cm^2/ V-s after NO annealing [63]. The mobility values near the bottom of the inversion layer of say 100 nm can be as high as 250 cm^2/ V-s [53] due to screening from the trapped electrons. If the trap density is

low, the number of trapped electrons will be lower and more of the inversion charges will be available to constitute the current. The effective mobility at the surface will thus be higher with lower trap densities. When the MOSFET works as a switch at a certain frequency of on and off, all the traps within the bandgap are involved with trapping and detrapping and therefore the complete characterisation of states within the bandgap is necessary. However, to study the effect of processing on mobility in an attempt to increase mobility, only the changes in trap density near or at the band edges can be studied where they are up to $10^{14}/cm^2$ eV, keeping in view that all the trap states from the CB edge to VB edge will be influenced by the processing. The electron mobility achieved by some research groups are summarised below in Table IV with the peak effective mobility of 265cm^2/V-s and a peak FE mobility of 154 cm^2/V-s achieved by Urresti et al.

Table IV. Effective and FE surface mobility and Hall bulk mobility of some n-channel 4H-SiC MOSFETs.

Reference	Sample P epilayer-Al doping, 4H-SiC-Si-face, (cm^{-3})	Oxidation	Annealing Conditions	Oxide thickness (nm)	Gate metal	Mobility (cm^2/V-s)
Chung et al. [63], 2001	1 x 10^{16} to 4 x 10^{16}	1100°C dry or wet with ROA	1175°C for 2 hrs. in NO	40	Mo	Effective mobility of 35
Dhar et al. [64], 2006	1 x 10^{16}	1150°C dry with ROA	1175°C for 2 hrs in NO followed by 500°C for 1 hr in H_2	45-55	Al or Au/Mo bilayer	Peak FE mobility of 45 after NO and 55 after NO + H_2 anneal
Poggi et al. [65], 2010	7.5 x 10^{15}	Two step—850°C for 30min +1100°C for 3-6 hrs.	N^+ implanted before ox	40-60	N^+ poly-Si	Hall effect mobility close to 100
Asaba et al. [66], 2018	5 x 10^{15}	CVD oxide	Pre-annealing in O_2 at less than 900°C + N_2 anneal at 1300°C for 1-10 hrs.	40-45	Unknown	Peak FE mobility of 50
Hatayama et al. [67], 2008	7.6 x 10^{15}	1-3 nm SiO_2 dry ox at 600-800°C + 70nm MOCVD Al_2O_3	No annealing	EOT of 30-35	Al	Peak FE mobility of 294, range is 200-300, mobility down to 40 with 2 nm SiO_2
Kang et al. [68], 2018	5 x 10^{15}	0.1-1nm La_2O_3+30nm ALD SiO_2	RTA in N_2O ambient at 900°C or 60s, Forming gas anneal 800°C for 5min	30	TaN capped with W	Peak FE mobility of 120 with 1nm La_2O_3
Noguchi et al. [69], 2019	3 x 10^{14} or 1 x 10^{16}	Thermally grown	1200°C for 1 hr in NO	5 and 50	P^+ implanted region	Phonon limited Hall mobility –over 100
Urresti et al. [70], 2019	5.3 x 10^{15}	About 1nm SiO_2 + ALD Al_2O_3	Dry ox by RTP at 600-800°C	40nm Al_2O_3 giving EOT of 29 nm	150nm Al	Peak effective mobility of 265 and peak FE mobility of 154

It can be observed from the Table IV above that three approaches have been applied to reduce the border trap density or NITs. In one approach, N is incorporated at the interface either by NO annealing or by N^+ implantation. NO annealing at 1175°C for 2 hrs increases the mobility from single digit to 35-45 cm^2/V-s [63, 64]. One main advantage of this method is that N is only at the interface and does not affect the bulk oxide. NO annealing followed by H_2 annealing further improves the mobility to55 cm^2/V-s [64]. Here, N passivates the C-related traps and H passivates the Si-dangling bonds at the surface bringing these states down to the VB edge or into it after passivation [51]. N^+ implantation followed by two step oxidation gives the Hall mobility of 100 cm^2/ V-s [65]. Asaba et al. [66] pre-annealed the CVD oxide in O_2 at less than 900°C and then N_2 annealed at1300°Cfor 1-10 hrs to give a peak FE mobility of 50 cm^2/V-s. The electrical integrity of this device is also very good with low low-field current density of 10^{-9} A/$cm^2$and high breakdown field of 9 MV/cm. One disadvantage that the author sees in N_2 annealing is that N_2 has high bond strength of 9.8 eV. It is difficult to break it down and requires more energy. It does not do any fresh oxidation as NO, not creating any new interface. It is similar to Chung's MOSFET with NO annealed oxide, which gives even higher mobility of 55 cm^2/ V-s with Dhar's forming gas anneal [64]. In the second approach by Hatayama et al. [67], a thin layer 1-3 nm SiO_2 with atomic layer deposited Al_2O_3 makes the gate stack. Since the border traps or NITs are known to be distributed in the 1-3 nm range, a 1 nm layer has less total NITs than a 2 or 3 nm thick oxide layer. Therefore a 1 nm SiO_2 gives a peak FE mobility of 294 cm^2/ V-s and increasing SiO_2 thickness to 2 nm reduces the mobility to 40 cm^2/ V-s because of larger total NITs [67]. In the third approach, NITs due to SiO_2 are completely eliminated by not having SiO_2. Instead, a 0.3 to 1 nm thick high-K La_2O_3 interlayer is used. After the ALD SiO_2 deposition, a post-deposition anneal in N_2O ambient is carried out by rapid thermal process for 60

s. This forms the lanthanum silicate and an SiO_x layer at the interface giving low total NITs. The forming gas anneal passivates only the Si-related interface traps at the La_2O_3/4H-SiC interface, giving a peak FE mobility of 120 cm^2/ V-s [68]. Noghuchi et al [69] repeated the first approach with NO annealing at 1200^oC for 1 hr that gave them the Hall bulk mobility close to 100 cm^2/ V-s. The second approach has been repeated by Urresti et al. [70] using Rapid Thermal Processing (RTP) to grow thin SiO_2 layer of 1 nm, giving peak effective mobility of 265 cm^2/V-s and peak FE mobility of 154 cm^2/V-s.

In this limited and essential discussion on mobility from the MOSFET application point-of-view, a suggestion to improve mobility is made. The trapping at NITs and other traps within the bandgap is the problem due to which the mobility is low where Coulomb scattering has been shown to dominate by looking at phonon-limited Hall bulk mobility [69]. In a summarised report by John Rozen [71], all the processing attempts to reduce trap density has been captured in one figure 10 presenting the D_{it} versus mobility trend. It can be observed that D_{it} reduces from $10^{12}/cm^2eV$ for as-grown to $10^{11}/cm^2$ eV for $POCl_3$ processing and increasing the field effect mobility from single digit to 90 cm^2 eV. Further reduction in D_{it} is required and attempts are being made. Inter-layers have their own problems of trapping charges between them and SiO_2 that degrades threshold voltage of the MOSFET due to BTI [61-62, 68]. A study by Hamadanian and Jabbari [72] shows that a surface treatment with ZnO for a TiO_2 based dye-sensitised solar cell, which forms a barrier layer can avoid recombination and increase electrons in TiO_2 CB. The interlayer high-K dielectrics develop bulk traps due to oxygen vacancies that act as border traps further away from the band edge at 0.048 eV [60].

A study by Pantelides et al. [73] compares Si/SiO_2 to SiC/SiO_2 and reports that while a totally abrupt interface is possible in Si/SiO_2 system, it is not favourable in SiC/SiO_2 system due to the hexagonal arrangement of atoms on SiC and so higher D_{it} and less abrupt interface of about 2 nm is present [40]. The author extends his view on this that from the long term reliability stand-point, all the compound semiconductors, such as SiC and GaN, will have the problem of less abrupt interface with more defects [74] that would trap charges and cause threshold voltage instability in devices due to BTI. However, the devices fabricated on them may capture niche markets like the SiO_2/HfO_2 gate stack in the HKMG technology and power devices such as BJT, MOSFET and JFETs on SiC having off-state voltage of 1200 V [75]. Ideally speaking, nothing can beat the Si/SiO_2 system, but the stacks also have reasonably high reliability by keeping the charge density between the SiO_2 and HfO_2 to around $10^{11}/cm^2$ and HfO_2 layer as amorphous through processing. Mean time-to-failure of over 100 years has been determined for devices with gate stacks.

G. Oxide Breakdown field and onset field for FN tunnelling

The oxide breakdown field must be studied along with the improvements in trap densities for higher mobility due to processing. While mobility may improve with different processing methods, the oxide breakdown field may reduce. The oxide breakdown field, E_{bd} can be determined from the FN tunnelling equation for a current density J, of approximately 10^{-4} A/cm^2, for thick oxides with thickness of tens of nanometres. The FN tunnelling equation is given [8, 18-19] as;

$$J = AE^2 \exp(-B/E) \qquad (16).$$

Here, E is the oxide field in MV/cm, B is the slope constant in the high field region of the I-V trace in MV/cm, and A is a constant in A/V^2. The onset field for FN tunnelling can be obtained at a current density of 10^{-8} A/cm^2. This 10^{-8} A/cm^2 is chosen by observing the leakage current at the onset of FN tunnelling in the p-type device which exhibits displacement current of the oxide capacitance only. There are no NITs at the VB edge. The n-type device has NITs at the CB edge and are lowering the leakage current to 8 x 10^{-13} A, which if divided by the dot area of 9.1 x 10^{-4} cm^2 gives a current density of 0.88 x 10^{-9} A/cm^2. This is approximated as 1 x 10^{-9} A/cm^2. This is the leakage current at the onset of FN tunnelling in the n-type device having NITs. Further calculations for this current density show that the onset field for tunnelling has reduced to 5.5 MV/cm (starting at 22 V for 40 nm oxide) with NITs from 5.8 MV/cm without NITs. These are presented in column 8 of second and first rows in Table V below. In other words, one is coming down the same slope to one order lower current and therefore the onset field is lowered. The low voltage electron and hole currents are also observed on Si-MOSFET of Eitan and Kolodny [76]. It can be observed in Fig. 2 of the reference that the hole current is 1.6 x 10^{-12} A at low gate voltages. The oxide capacitance for the 8.5 nm thick oxide having a C-V dot area of 1.6 x 10^{-4} cm^2 is 65 pF. The displacement current calculated for the ramp rate of 0.1 V/s is 6.5 x 10^{-12} A, giving a current density of 4 x 10^{-8} A/cm^2. This is the displacement current of the oxide capacitance only. The observed hole current of 1.6 x 10^{-12} A gives a current density of 10^{-8} A/cm^2. This is 4 times lower than the oxide displacement current because the p-type substrate is in inversion and not in accumulation across the oxide. In inversion, the capacitance is lowered because of substrate depletion capacitance, thereby giving lower current based on the equation (13). The electron current is only across the oxide. The electron current density at low voltage is 5 x 10^{-10} A/cm^2 which is two orders lower than the oxide displacement current of 4 x 10^{-8} A/cm^2. It

indicates the presence of NITs near the CB of Si which are getting charged and lowering the current as in 4H-SiC described earlier. The D_{NIT} for Si is determined to be 12 x 10^{11}/cm^{2}eV by the method presented in sub-section E. The onset field with NITs is reduced to 6.5 MV/cm from 7.2 MV/cm without NITs. The observed onset field in Fig.2 of reference [76] for the electron current after voltage correction [19] is 5.5 V for the 8.5 nm oxide which is equal to 6.4 MV/cm. The observed and calculated onset field for electron tunnelling current is the same. There are no NITs at the VB edge of both Si and 4H-SiC and the trap density is represented only by D_{it}.

Table V. Barrier height dependent breakdown field and onset field for FN tunnelling in SiO_2 on 4H-SiC and on Si due to electrons and holes.

Sample Type (accumulation) SiO_2 on 4H-SiC and on Si	Factor A (x 10^{-6}) A/V^2	CBO and VBO with 4H-SiC and Si (eV)	Current density J at E_{bd} (x 10^{-4}) A/cm^2	Slope constant B (MV/cm)	Barrier height dependent breakdown field in SiO_2, E_{bd} (MV/cm)	Low voltage leakage current density (A/cm^2) x 10^{-8}	Barrier height dependent FN onset field (MV/cm)	Density of border traps or NITs (cm^{-2}eV^{-1}) x10^{11} at 300K
n-4H-SiC, [8]	1.31	CBO =2.8	2.7	206	7.8	1.0 (taken)	5.8 without NITs at CB	0
n-4H-SiC, [8]	1.31	CBO=2.8	2.7	206	7.8	0.1 (observed)	5.5 with NITs at CB	23.5
n-Si, [19]	1.15	CBO=3.2	2.2	254	9.5	4.0 (taken)	7.2 without NITs at CB	0
n-Si, [19, 76]	1.15	CBO=3.2	2.5	254	9.5	0.05 (observed)	6.5 with NITs at CB	12
p-4H-SiC, [18]	0.92	VBO =2.9	1.3	258	9.5	1.0 (observed)	7.2 no NITs at VB	0
p-Si, [19, 76]	0.58	VBO =4.6	0.74	514	18.0	4.0 (taken)	14.0 without NITs at VB	0

The slope constants obtained for the electron and hole conduction are with the oxide fields corrected for the flat band voltages [18]. The breakdown fields from the works of Williams et al. [51] are not having oxide fields corrected for flat band voltages and therefore the oxide breakdown fields in Williams et al. [51] are lower for p-type devices having hole conduction even when the VBO is 0.1 eV larger than CBO. The n-type devices have negligible flat band voltages after NO annealing with oxides grown and having ROA included. It can be observed in Table V above, that the breakdown field and onset field for FN tunnelling in SiO_2 on 4H-SiC is lower than that on Si for both carrier types and with and without NITs.

H. Interrelated Current-Voltage and low and high frequency Capacitance-Voltage traces in a MOS device

The oxide breakdown field is obtained from the current-voltage curve. The oxide is said to be in breakdown condition when the current density reaches 10^{-4} A/cm^2 in thick oxides of tens of nanometres. The oxide voltage is corrected by the flat band voltage, and the flat band voltage is obtained from the high frequency C-V trace [8, 18]. The breakdown field is obtained from the slope constant B, of the high-field I-V trace and needs to be corrected by the amount of charges in the oxide represented by the flat band voltage. This is the first interrelation. The low voltage leakage current density in the MOS device reduces below the true oxide leakage current density of 10^{-8}A/cm^2 for the oxide on 4H-SiC, because of trapping electrons in the NITs at the CB edge. This has been elaborated in the sub-section E. The observed low current density can provide the capacitance of NITs at 300K from equation (13). The capacitance can give the density of the traps at 300K, which can be further extrapolated to 1K temperature by lowering the average electron energy and thus coming closer to the CB edge. Thus the distribution of the D_{NIT} in sub-0.026 eV from the CB edge can be obtained. Here, the leakage current is related to the low frequency C-V trace. This is the second interrelation.

Table VI. Displacement current density in SiO_2 on 4H-SiC and on Si at 300K

Semiconductor	Capacitance of SiO_2 (pF)	Leakage current in SiO_2 From eqn (13) and ramp rate of 0.1 V/s, (A)	C-V dot area (cm^2)	Displacement Current density in SiO_2 (A/cm^2)	Thickness of SiO_2 (nm)	Ratio of oxide displacement current density Si/SiC	Ratio of oxide thickness SiC/Si
n-4H-SiC, [8]	80	8 x 10^{-12}	9.1 x 10^{-4}	0.88 x 10^{-8}	40	4.6	4.7
p-Si (inversion) , [76]	65	6.5 x 10^{-12}	1.6 x 10^{-4}	4.06 x 10^{-8}	8.5		

The Table VI above presents the displacement current density in SiO_2only. It is an important starting point for the analysis of an I-V trace on a MOS device. The main argument is that, if the observed low field leakage current is more than the displacement current of the oxide in accumulation or inversion, then, there are defects in the oxide that need to be cured such that the oxide is more amorphous and free of charges. If the observed current is less than the displacement current in the oxide, then there are charges trapped at the interface states or border traps (NITs) that need to be passivated by processing or completely removed. The observed majority carrier current being less than the displacement current for the device does not always mean that there are NITs present. It could be that an inverted device like the n-channel Si MOSFET [76] is in depletion lowering the total capacitance and therefore the majority carrier current. For example, the majority hole current density at low fields is 10^{-8} A/cm^2 when the displacement current density is 4 x 10^{-8} A/cm^2 in the n-channel MOSFET as can be observed in Fig. 2 of the reference [76]. The high field current-voltage characteristics will yield the breakdown field strength. It is found to be related to the charges in the oxide that can influence the slope constant B, and consequently the oxide breakdown field and onset field for FN tunnelling.

In view of the above argument, I-V traces before and after forming gas annealing in the gate stack of the n-channel 4H-SiC MOSFET by Kang et al. [68] having a 0.3 nm La_2O_3 layer is analysed. The device has an ALD SiO_2 mainly of 30 nm and the active area is 4 x 10^{-4} cm^2. This gives the oxide capacitance of 46 pF. The displacement current for the oxide comes out to be 4.6 x 10^{-12} A for the ramp rate of 0.1 V/s, or a displacement current density of 1.15 x 10^{-8} A/cm^2. It is observed that the low voltage current density is 2.5 x10^{-7} A/cm^2, one order more than the displacement current density. It implies that the bulk has a high defect density. The breakdown field is also much lower than 7.8 MV/cm at only 4.0 MV/cm at 10^{-4}A/cm^2 because of high bulk defect density. The interface trap density is reduced after forming gas annealing so as to improve mobility, and so the leakage current density comes closer to the displacement current density, but it is still high at 5 x 10^{-8} A/cm^2 because of the high number of bulk defects. The breakdown also improves a little bit to 4.5 MV/cm, but it is still very low. It is therefore the author's opinion that studies on the MOS device should be done with both I-V/C-V interrelated curves, and not only I-V and only C-V curves. For example, the D_{it} may be lowered at the interface after processing which is obtained from the C-V curves like in the Kang et al. [68], but the oxide breakdown fields may reduce due to too many bulk defects in the oxide or the gate stack used. This can be done simply by observing the I-V trace at low and high fields relative to the displacement current as described above. For the device of Kang et al., the bulk defect density has to be improved more now after reducing trap density to improve mobility by forming gas annealing. If the density of bulk traps is reduced, the dielectric capacitance will reduce, effectively increasing the thickness and thereby reduce the vertical field or effective field to increase the FE mobility further. This happens when the thickness of the La_2O_3 is increased from 0.3 nm to 1 nm, and post deposition annealing at 900^{o}C in pure N_2O ambient by rapid thermal process is performed. The annealing is making the ALD SiO_2 more amorphous and defect free as shown by the XPS diagram also. The peak FE mobility increases from 45 to 120 cm^2/ V-s [77]. It goes down to about 80 cm^2/ V-s with increased vertical field. The interface trap density is still high at 2 x 10^{12}/cm^{2}eV at E_c-0.2 eV. The D_{it} for the NO annealed sample of Williams et al. [51] is 8 x 10^{11}/cm^2 eV at E_c-0.2 eV and is comparatively less than above. The O from La_2O_3 is forming a SiO_x layer after post-deposition anneal at 900^{o}C giving less total NITs that dominate the mobility increase rather than the D_{it} at E_c-0.2 eV. One should therefore be looking at the border trap density (NITs) which are much closer to the CB edge than D_{it} atE_c-0.2 eV. The dielectric breakdown strength is also good at 8 MV/cm for a current density of 10^{-4} A/cm^2. The O appears to be a good alternative for giving reduced total NITs by the formation of SiO_x at the interface.

I. Which atom can give lower border trap density---N or O? and finally H in both

The last part of the above analysis clearly indicates that the focus should be on the D_{NIT} (same as D_{bt}) values in the oxide near CB of 4H-SiC and Si pointing to the two values of 23.5 x 10^{11}/cm^{2}eV for 4H-SiC and 12 x 10^{11}/cm^{2}eV for Si at 300 K. Only the oxide on SiC is NO annealed. The border trap density on SiC is twice that on Si. Nitrogen and Oxygen both can be used to remove Carbon from the SiC/SiO_2 interface. If N is used it binds to C and shifts the energy state to the VB edge [51]. N at the saturation level of about 10^{21}/cm^3 removes all C [40] and the interface is new with N. The density of NITs is now given as 23.5 x 10^{11}/cm^2 eV representing Si-N and Si-ON bonds as given above. This nitride is on SiC and has about 10 times higher D_{bt} than those determined for Jet Vapour Deposited (JVD) nitride on Si. The border trap density for JVD Nitride on Si has been obtained to be 8 x 10^{10}/cm^{2}eV to 4 x 10^{11}/cm^{2}eV [78]. If O is used as in Yang et al. [77] discussed above, it can give a reduced total NITs closer to CB edge by forming a very thin layer of SiO_x. It is observed that N inclusion is not improving the mobility as much as by growing a 1 nm thick $SiO_2$for reduced total NITs [67, 70] or forming SiO_x by taking O from La_2O_3 after post deposition anneal at 900^{o}C [68, 77]. Growing 1 nm SiO_2, or forming SiO_x by taking O from La_2O_3 may include some C. In the author's opinion, O could be used as above to reduce total NITs. O is definitely doing a better job than N in reducing total NITs. This is ascertained by observing the peak FE mobility obtained in the MOSFETs of Table IV. Two questions come to

mind. One, how can N reduce border trap density further? Second, how stable is the SiO_x layer or 1 nm SiO_2 layer? It needs to be mentioned here that after forming gas anneal, the D_{it} in MNS structure is in low 10^{11} order [79], whereas in MOS device it is in low 10^{10} order near midgap. JVD nitride also has more bulk defects than SiO_2. One can learn from the works on JVD nitride that nitride is not as good as SiO_2. This is known from the Si technology. The possibility of O beating N is higher. One example to this assertion is the observation of pre-stress I_{DS}-V_{GS} traces on Si MOSFET and MNSFET in Fig. 1 of reference [80]. The MOSFET has a slightly better effective mobility. Finally, forming gas (10% H_2 + N_2) anneal at 450^{o}C to 500^{o}C for 30 to 60 minutes can reduce D_{bt} in both N and O containing interface by passivating Si dangling bonds, as shown in the works of Dhar et al. [64].

The density of border traps, D_{bt} in SiO_2/Si system is obtained above as 12 x 10^{11}/cm^{2}eV by the author at 300 K. D_{bt} for the amorphous HfO_2/SiO_2 gate stack of HKMG MOSFET is also the same. The stack has an EOT of 1.4 nm. The D_{it} further away from the CB edge is one order lower in as deposited ALD HfO_2, annealed at 600^{o}C in Ar, and exposed to dc H plasma. It has an acceptable threshold voltage shift under long time low voltage bias stress conditions. This is the brief learning take away from two studies [81, 82]. They corroborate the author's calculation of D_{bt} or D_{NIT} on the SiO_2/Si system and the new method of determination from observation of low field leakage current with MOS device in accumulation or inversion.

J. Some special qualification points

Few points are added to qualify the previous sub-sections:

1. The formula for average D_{NIT} or D_{bt} presented in equation (15) can be applied up to 575 K temperature giving average electron energy of about 0.05 eV from the CB edge and is applicable for thick oxides greater than 7-8 nm having low low-field leakage current in accumulation.
2. At low temperature of 1.5 K, the electron surface mobility is found to decrease with electron concentration above 10^{11}/cm^2 or 10^{16}/cm^3, assuming a 100 nm channel, when the semiconductor starts behaving like a two dimensional metal [83]. This limitation needs to be kept in mind while using equation (15) for D_{NIT}. In other words, the formula in equation (15) can be limited for use to 10 K temperature instead of 1 K and can still be almost at the band edge, about 0.001 eV away.
3. I_d-V_{gs} or C-V hysteresis curves [55, 78, 84] provide trap densities away from the band edges and are therefore lower than those obtained by the equation (15) at 300 K, but can be applied to MOSFETs having thin oxides of 3 nm also [78].
4. Use of ZnO barrier layer with 4H-SiC may lead to deep level defect formation with Zn in 4H-SiC, after the O is removed to form SiO_x layer on 4H-SiC with processing. Instead, ozone oxidation from room temperature to less than 600^{o}C may be better to form 1 nm SiO_2 layer on 4H-SiC [85-86]. Two atoms of O will combine with Si to form SiO_2 and the third atom will remove C from 4H-SiC by forming CO. Interlayer charge density between this 1 nm SiO_2 and the oxide above it have to be kept low around 10^{11}/cm^2 for reduced bias stress instability of the threshold voltage of the MOSFETs [87].

IV. Conclusion

Two new ideas form part of this article. First, the derivation of average oxide fields for carrier tunnelling across the MOS devices in accumulation has been presented. Second, the density of NITs or border traps in the oxide near the CB of n-4H-SiC and Si MOS device has been determined from the low field leakage current. D_{NIT} or D_{bt} at the CB edge of 4H-SiC after NO annealing is 23.5 x 10^{11}/cm^{2}eV and at the CB edge of Si is half of that at12 x 10^{11}/cm^{2}eV at 300K. The concern about N incorporation in the oxide due to NO annealing causing error in the MOS characterisation has been clarified. N is incorporated at the SiC/SiO_2 interface only, after NO annealing. Both, the dry and wet oxidation followed by N incorporation at the interface of 4H-SiC/SiO_2 to the saturation level, reproduce the same V_{fb} results, provided ROA is part of the oxide growth process. However, NO annealing reduces the D_{it} at the SiC/SiO_2 interface by one order. The data of flat band voltage is found to be reproducible after correcting for work function differences of different gate metals used in the study. The oxide thickness needs to be exact and has been proven to be correct as 40 nm by the fact that the CBO of 2.78 eV for the Si-face of n-type device has been reproduced by other groups. Near Interface Traps (NIT) or border traps exists in the oxide only near the CB of 4H-SiC and in oxide on Si near CB edge and not near the VB edge where traps are represented by D_{it}. NBTI will cause degradation in the threshold voltage of the p-channel MOSFET, and PBTI will degrade the threshold voltage of the n-channel MOSFET. The barrier height dependent breakdown field and onset field for FN tunnelling in SiO_2 is lower on 4H-SiC than on Si for both electrons and holes as current carriers. The article strengthens and improves the credibility of the author's earlier studies of MOS characterisation. Low and high power MOSFET technology development is the application of the present article where reducing the density of near interface traps would increase the carrier mobility and hence current in the device of the same dimensions. The dielectric leakage and breakdown

strength should also be acceptable while improving mobility in the MOSFETs. Observing the low field leakage current relative to the displacement current of the oxide informs us about the D_{NIT}, same as D_{bt} (density of border traps) and the high field current informs us about the bulk defect density and the dielectric breakdown strength and onset field for FN tunnelling. The oxide charges and the metal-semiconductor work-function difference represented by the flat band voltage affects the high field I-V trace and the slope constant. There is a tussle between N and O, as to which can give lower D_{bt} so as to give higher surface mobility, and finally H passivates the Si-bonds in both, SiC and Si. The qualification points of sub-section J are important. BTI in the threshold voltage of the MOSFETs cannot be completely eliminated, but can be kept low.

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